

Floorplanning Cheat Sheet

♦ What Is Floorplanning?

- First major physical design step after synthesis
 - Defines chip's physical organization
 - Impacts: Timing | Power | Area | Routability
 - Foundation for placement → CTS → routing
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Key Objectives

Objective	Description
Define Core Area	Based on die size, utilization, std. cells/macros
Place Macros	Memories, IPs, with orientation + spacing
IO Placement	Input/output pads/bumps (wirebond/flip-chip)
Power Planning	Rings, stripes, mesh
Channel Planning	Leave whitespace between macros
Clock Planning	Place FF-heavy logic for easier CTS
Define Blockages	Restrict placement near macros/analog blocks

Inputs to Floorplan

- Synthesized netlist (.v) → logic hierarchy
 - Constraints (SDC) → timing
 - Tech LEF → std. cell + macro sizes
 - Power intent (UPF/CPF) → multi-V, low power
 - IO Pad Ring → pad definition (wirebond)
 - Macro LEF/DEF → orientation + pins
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Floorplanning Flow

1. Estimate die/core area (utilization)
 2. Define core boundary (core-to-die ratio)
 3. Place hard macros / analog IPs
 4. Place IO pads/bumps
 5. Reserve whitespace & channels
 6. Create power planning (rings/stripes)
 7. Add blockages (hard/soft)
 8. Define regions/partitions (optional)
 9. Verify DRC, overlaps, accessibility
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Important Metrics

Parameter	Description
Core Utilization	Std. cell area ÷ core area (60–80%)
Core-to-Die Ratio	Core vs die edge spacing
Aspect Ratio	W:H (ideal $\approx$ 1:1)
Halo	Keep-out margin around macros
Channel Spacing	Space between macros
Row Utilization	% of std. cell rows used

Macro Placement Best Practices

- Place large macros near edges → better routing & isolation
- Avoid corners → routing restriction
- Orient for pin accessibility → fewer detours
- Leave channels between macros → avoid congestion
- Use halo + blockages → prevent close placement

Power Planning (During Floorplan)

- Power Rings: around core/macros, wide metals
- Stripes: inside core (H/V)
- Tap Cells: tie substrate to power net
- Well Taps + Decaps: noise stability
- Domain Separation: for multi-V (UPF/CPF)

Floorplan Constraints (Tool-Level)

Constraint	Purpose
Soft Blockages	Block placement (routing allowed)
Hard Blockages	Block both placement + routing
Region Constraints	Force logic into area
Fence Region	Boundary for IP reuse
Pin Constraints	Guide IO/macro pin placement

Tool Commands

Cadence Innovus

```
floorPlan -site CORE -coreUtil
0.7 -aspectRatio 1.0 -coreToDie
2
placeIoPins
addHalo -allMacros -halo 10 10
10 10
createPlaceBlockage -type hard
-area {x1 y1 x2 y2}
```

Synopsys ICC2

```
initialize_floorplan
-utilization 0.7 -aspect_ratio
1.0
create_power_straps
create_macro_blockage -region
{x1 y1 x2 y2}
```

Timing violations	Bad macro location	Move logic closer, reroute
Power DRCs	Stripe/ring issues	Redo with correct pitch/width
Routing detours	Poor pin access	Adjust orientation, constraints

Post-Floorplan Checks

- DRC clean (no overlaps/spacings)
- Power/ground rings + stripes present
- Clock sinks distributed well
- No macros in corners / bottlenecks
- IR/EM preview (RedHawk/Voltus)

Common Issues & Fixes

Issue	Cause	Fix
Macro overlaps	Bad placement/ halo	Reposition + set halo
Congesti on zones	Dense macros	Increase spacing, add channels